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TECHNICAL GUIDE

Catching BMS Controller Failures Before They Reach Your Site

How disciplined Factory Acceptance Tests (FAT) and Site Acceptance Tests (SAT) eliminate 80–90% of commissioning faults — and slash project costs.

EnSmart Building Automation · Pune Project Insight · 2024 · bmssales@ensmart.ai

The Incident That Started This Guide

A 28-controller BMS panel ships from a factory in Erode to a pharma plant in Pune. Commissioning begins Wednesday. By Friday, three controllers will not talk to the front-end. The panel team blames the network. The customer blames the panel.

Controller	Fault Found On-Site	Time Lost
Controller 7	BACnet device-instance conflict	2 hours
Controller 14	Wrong baud rate configured at factory	1 hour
Controller 22	DIP switch position incorrect	30 minutes

Root cause: None of these faults had been tested at the factory. The factory test verified power-on, basic comms, and IO continuity — but never ran the controllers as a live network with their actual configuration.

The Cost of Finding Faults Late

3
Senior-engineer days lost on-site

2 Days
Project schedule slipped

2 Hours
Same faults fixed at factory bench

> *Catching faults early is one of the highest-leverage things a BMS project can do. The earlier the catch, the cheaper the fix.*

FAT — Factory Acceptance Test

Where: At the panel manufacturer's factory, before shipment. **When:** After panel build is complete and before crating. **Who:** Vendor's test engineer + customer witness representative.

Output: Signed FAT report, photographs, configuration backups.

STEP 01	**Visual Inspection**	Panel construction matches drawing (IP rating, dimensions, colour). Component placement matches layout drawing. Wiring tidy and labelled. Earthing continuity verified.
STEP 02	**Power-On Test**	Apply 230V or 24V per panel design. Confirm no sparks, smoke, or alarms. Confirm SMPS output voltages within tolerance. Fan/cooling operation verified.
STEP 03	**Controller Boot Verification**	Each controller boots to firmware. Device instance, IP address, baud rate, and MAC address verified against the configuration document. PICS/BIBB profile confirmed.
STEP 04	**IO Point-to-Point Continuity**	Test signal applied to each AI input — controller reading confirmed. Each DI toggled — controller reading confirmed. Each DO commanded — relay actuates. Each AO commanded — voltage confirmed at terminal. Every channel documented in FAT report.
STEP 05	**Network Communication**	Every controller discoverable from supervisor via BACnet. Every Modbus device discoverable on its assigned chain. End-to-end ping confirmed from front-end to each controller.
STEP 06	**Sequence Sample Testing**	For at least 3 controllers: simulate inputs and verify FBD logic produces correct outputs. For chiller plant: simulate full sequence — start, stage, trip, restart.
STEP 07	**Configuration Backup**	JSON or vendor-format backup taken for every controller. Saved to project folder and copied to USB for handoff.
STEP 08	**Signed FAT Report**	Test engineer signs each section. Customer witness countersigns. Two copies retained — one with vendor, one with customer.

FAT Duration: A thorough FAT for a 28-controller panel takes 2–3 days.

It catches 80–90% of configuration errors before the shipment leaves the factory. This is the single highest-leverage investment in any BMS project.

SAT — Site Acceptance Test

Where: At the customer's site, after panel installation and cable termination. **When:** After all field wiring is complete and before handover. **Who:** Vendor + integrator + customer + (for regulated sites) consultant.

Output: Signed SAT report, photographs, as-built drawings.

STEP 01	**Site Visual Inspection**	Panel installation matches design drawing. Cable termination matches IO list. Cable routing matches drawing. Earthing tested at panel.
STEP 02	**Field-End IO Verification**	Known input applied at the field sensor (heat the temp sensor, open the DPS, depress the limit switch). BMS dashboard confirms correct value. Repeated for every IO point — every single one. Every channel documented.
STEP 03	**Sequence Verification**	Every sequence run end-to-end: chiller staging, AHU start, fire mode, occupancy mode, schedule transitions. Alarms verified. Trends confirmed recording.
STEP 04	**Network Verification**	Front-end discovers all controllers. Front-end can read and write every IO point. COV subscriptions functioning for high-priority points. BACnet routing confirmed across all networks.
STEP 05	**Failover and Edge Cases**	Lead pump tripped — lag promotes correctly. Sensor disconnected — alarm generated. Controller power-cycled — recovery confirmed. Network cable disconnected — graceful degradation verified.
STEP 06	**Operator Training**	Walk-through of front-end with operators. Alarm queue review. Trend access. Schedule modification. Emergency override procedures documented.
STEP 07	**Documentation Handover**	As-built drawings (red-marked from design). Final IO list including field changes. Sequence of operations. Alarm and event list. Maintenance schedule. Configuration backups.
STEP 08	**Signed SAT Report**	Each section signed by vendor and customer. Open-issues list with timelines. Final acceptance signed when all open issues are closed.

SAT Duration: Typically 3–5 days for a 28-controller panel.

SAT catches the remaining 10–20% of issues that survived FAT — particularly field wiring errors, sensor calibration issues, and sequence edge cases that only appear with real building loads.

What Pharma 21 CFR Demands From Both FAT and SAT

For pharma sites, FAT and SAT take on additional regulatory weight under 21 CFR. Each test must be witnessed, signed, time-stamped, and retrievable for FDA inspection up to 7 years. Any deviation must be formally documented and resolved.

Witnessed by qualified person	Customer + vendor + QA must all be present and sign.
Signed, time-stamped records	Every test step recorded with timestamp and signature.
References the URS	Each test must trace back to the User Requirements Specification.
7-year retrievability	Records must be accessible for FDA inspection up to 7 years.
Formal deviation reports	Any deviation documented and resolved with formal process.
Validation lifecycle tie-in	FAT/SAT linked to URS, FDS, IQ, OQ, PQ documentation.

Additional Pharma FAT Requirements

- Validation protocol verification against approved IQ/OQ protocols
- 21 CFR Part 11 audit trail testing — every user action logged
- Electronic signature workflow testing end-to-end
- Data integrity testing — read consistency, tamper detection
- Backup and recovery testing with verified restoration

After Reworking the FAT Process — Measured Results

Following the Pune incident, the factory reworked its FAT process with a 3-day system test added to scope, all controllers tested as a live network, sample sequences run from the supervisor, and configuration backups taken before crating. Customer witness invited to every FAT. FAT signoff required before crating.

80%	40%	5 → 1
Reduction in site commissioning faults	Reduction in average commissioning duration	Average faults per project (before vs after)

> *The factory's reputation became the reputation for clean, predictable, on-time delivery — because what shipped from the factory was actually tested, not just assembled.*

Work with EnSmart on Your Next BMS Project

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